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09/846,301	05/02/2001	Takashi Horiyama	0033-0720P	3874

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EXAMINER	
GOLE, AMOL V	

ART UNIT	PAPER NUMBER
2183	4

DATE MAILED: 02/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/846,301	HORIYAMA ET AL.	
	Examiner	Art Unit	
	Amol V. Gole	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file:

#2: Priority (5/2//01)

#3: IDS (5/2/01)

Information Disclosure Statement

3. The IDS form 1449 submitted by the applicant indicates the translation of the abstract of the foreign patent No. a683731 to be provided. However no such translation was provided. According to the applicant's IDS, the relevancy of this document is to be determined from the English abstract. However, as the English abstract and hence relevancy is not provided, this document will not be considered by the examiner.

Specification

4. The abstract of the disclosure is objected to because it does not provide a sufficient description of the claimed invention. Correction is required. See MPEP § 608.01(b).

5. The disclosure is objected to because of the following informalities:

1) pg. 6, line 7, please change "PE1->PE1->PE->PE2" to "PE1->PE1->**PE3**->PE2".

2) pg. 6, line 12, please change "5r->router 5->5c" to "**5e**->router 5->5c".

3) pg. 17, line 21, please insert the word "may" between the words "or not" for grammatical reasons.

4) pg. 17, lines 24-25, it is mentioned the junction unit 15a is formed by (M-1) 2-input, 1-output junction units. Please elaborate on this for purposes of understanding the invention.

5) pg. 18, line 3, please change "M-times" to "N-times" transfer rate to correctly reflect the invention.

6) pg. 18, line 31, please change "relay" to "delay".

Appropriate correction is required.

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: DATA DRIVEN TYPE APPARATUS AND METHOD WITH ROUTER OPERATING AT A DIFFERENT TRANSFER RATE THAN SYSTEM TO ATTAIN HIGHER THROUGHPUT.

Claim Objections

7. Claims 5 and 10 are objected to because of the following informalities: Please insert a "the" between the words "is larger" for grammatical purposes. Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims **1-10** are rejected under 35 U.S.C. 102(b) as being unpatentable over the admitted prior art of pages 1-11 of the applicant's background.

10. In regard to claim 1:

11. The applicant's background discloses a method of controlling execution of a data driven type information processing apparatus (fig 12, fig. 19) including

a router (fig. 19) including an M-input (fig. 19, 2-input), 1-output junction unit (fig. 19, 11a) and a 1-input, N-output (fig. 19, 2-output) branching unit (fig. 19, 11b), controlling input/output of a data packet (pg. 6, lines 2-13 disclose that the router's function of controlling input/output of a data packet) including at least a destination node number (fig. 6, F1), an instruction code (fig. 6, F3), and data (fig. 6, F4), and

a self-synchronous transfer control circuit (fig. 7, 1a; pg. 2, lines 5-7) generating a transfer request signal (SEND signal is sent from pulse output terminal C0, pg. 3, lines 10-16) and transfer acknowledge signal (ACK signal is sent from pulse output terminal R0, pg. 3, lines 10-16) controlling transfer and operating processes of said data packet (clock pulse CP is provided to control the data holding operation; pg. 2, lines 13-15), wherein

transfer rate used in the self-synchronous transfer control circuit (the self-synchronous transfer control circuit controls the data transfer rate depending on preset delay time; pg. 3, lines1-7) in said router is made different from the transfer rate used in a system (pg. 9, lines 24-33 and pg. 10, line 1 disclose that the transfer rate of the

router path 11c is equal to or greater than the sum of the system transfer rates of the two inputs, therefore making it different from the transfer rate used in the system).

12. In regard to claim 2:

13. Applicant's background further discloses the method of controlling execution of a data driven type information processing apparatus according to claim 1, wherein the transfer rate used in said self-synchronous transfer control circuit of said router is a multiplication of the transfer rate used in said system (pg. 9, lines 24-33 and pg. 10, line 1 disclose that the transfer rate of the router path 11c is equal to or greater than the sum of the system transfer rates of the two inputs, therefore making it a multiplication of the transfer rate used in the system).

14. In regard to claim 3:

15. Applicant's background further discloses the method of controlling execution of a data driven type information processing apparatus according to claim 1, wherein the transfer rate used in said self-synchronous transfer control circuit of said router is a total sum of transfer rates of inputs to said router (pg. 9, lines 24-33 and pg. 10, line 1 disclose that the transfer rate of the router path 11c is equal to the sum of the system transfer rates of the two inputs).

16. In regard to claim 4:

17. Applicant's background further discloses the method of controlling execution of a data driven type information processing apparatus according to claim 1, wherein the transfer rate used in said self-synchronous transfer control circuit of said router is a total sum of transfer rates of outputs from said router (pg. 9, lines 24-33 and pg. 10, line 1 disclose that for the configuration in fig. 19 where the number of inputs is equal to the number of outputs, the transfer rate of the router path 11c is equal to the sum of the transfer rates of the two inputs. However, the outputs are connected to processing elements (fig. 12, PE1-PE4) having the same self-synchronous transfer control circuits (fig. 11, 2a-2c) and hence same transfer rates. Therefore, although not explicitly mentioned, it is deemed inherent that the transfer rate of the router path 11c is equal to the sum of the system transfer rates of the two outputs also because they have the same transfer rates as the inputs).

18. In regard to claim 5:

19. Applicant's background discloses the method of controlling execution of a data driven type information processing apparatus according to claim 1, wherein the transfer rate used in said self-synchronous transfer control circuit of said router is the larger one of the total sum of the transfer rates of the inputs to said router and the total sum of the transfer rates of the outputs from said router (pg. 9, lines 24-33 and pg. 10, line 1 disclose that for the configuration in fig. 19 where the number of inputs is equal to the number of outputs, the transfer rate of the router path 11c is equal to the sum of the

system transfer rates of the two inputs. However, the outputs are connected to processing elements (fig. 12, PE1-PE4) having the same self-synchronous transfer control circuits (fig. 11, 2a-2c) and hence same transfer rates. Therefore, although not explicitly mentioned, it is deemed inherent that the transfer rate of the router path 11c is equal to the sum of the system transfer rates of the two outputs also because they have the same transfer rates as the inputs. As both the totals of the transfer rates of the inputs and outputs are the same the transfer rate of the router is effectively equal to the larger one).

20. In regard to claim 6:

21. The applicant's background discloses a data driven type information processing apparatus (fig 12, fig. 19) comprising:

a router (fig. 19) including an M-input (fig. 19, 2-input), 1-output junction unit (fig. 19, 11a) and a 1-input, N-output (fig. 19, 2-output) branching unit (fig. 19, 11b), controlling input/output of a data packet (pg. 6, lines 2-13 disclose that the router's function of controlling input/output of a data packet) including at least a destination node number (fig. 6, F1), an instruction code (fig. 6, F3), and data (fig. 6, F4), and

a self-synchronous transfer control circuit (fig. 7, 1a; pg. 2, lines 5-7) generating a transfer request signal (SEND signal is sent from pulse output terminal C0, pg. 3, lines 10-16) and transfer acknowledge signal (ACK signal is sent from pulse output terminal R0, pg. 3, lines 10-16) controlling transfer and operating processes of said data packet

(clock pulse CP is provided to control the data holding operation; pg. 2, lines 13-15), wherein

transfer rate used in the self-synchronous transfer control circuit (the self-synchronous transfer control circuit controls the data transfer rate depending on preset delay time; pg. 3, lines1-7) in said router is made different from the transfer rate used in a system (pg. 9, lines 24-33 and pg. 10, line 1 disclose that the transfer rate of the router path 11c is equal to or greater than the sum of the system transfer rates of the two inputs, therefore making it different from the transfer rate used in the system).

22. In regard to claim 7:

23. Applicant's background further discloses a data driven type information processing apparatus according to claim 6, wherein the transfer rate used in said self-synchronous transfer control circuit of said router is a multiplication of the transfer rate used in said system (pg. 9, lines 24-33 and pg. 10, line 1 disclose that the transfer rate of the router path 11c is equal to or greater than the sum of the system transfer rates of the two inputs, therefore making it a multiplication of the transfer rate used in the system).

24. In regard to claim 8:

25. Applicant's background further discloses a data driven type information processing apparatus according to claim 6, wherein the transfer rate used in said self-synchronous transfer control circuit of said router is a total sum of transfer rates of inputs to said router (pg. 9, lines 24-33 and pg. 10, line 1 disclose that the transfer rate of the router path 11c is equal to the sum of the system transfer rates of the two inputs).

26. In regard to claim 9:

27. Applicant's background further discloses a data driven type information processing apparatus according to claim 6, wherein the transfer rate used in said self-synchronous transfer control circuit of said router is a total sum of transfer rates of outputs from said router (pg. 9, lines 24-33 and pg. 10, line 1 disclose that for the configuration in fig. 19 where the number of inputs is equal to the number of outputs, the transfer rate of the router path 11c is equal to the sum of the transfer rates of the two inputs. However, the outputs are connected to processing elements (fig. 12, PE1-PE4) having the same self-synchronous transfer control circuits (fig. 11, 2a-2c) and hence same transfer rates. Therefore, although not explicitly mentioned, it is deemed inherent that the transfer rate of the router path 11c is equal to the sum of the system transfer rates of the two outputs also because they have the same transfer rates as the inputs).

28. In regard to claim 10:

29. Applicant's background discloses a data driven type information processing apparatus according to claim 6, wherein the transfer rate used in said self-synchronous transfer control circuit of said router is the larger one of the total sum of the transfer rates of the inputs to said router and the total sum of the transfer rates of the outputs from said router (pg. 9, lines 24-33 and pg. 10, line 1 disclose that for the configuration in fig. 19 where the number of inputs is equal to the number of outputs, the transfer rate of the router path 11c is equal to the sum of the system transfer rates of the two inputs. However, the outputs are connected to processing elements (fig. 12, PE1-PE4) having the same self-synchronous transfer control circuits (fig. 11, 2a-2c) and hence same transfer rates. Therefore, although not explicitly mentioned, it is deemed inherent that the transfer rate of the router path 11c is equal to the sum of the transfer rates of the two outputs also because they have the same transfer rates as the inputs. As both the totals of the transfer rates of the inputs and outputs are the same the transfer rate of the router is effectively equal to the larger one).

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

31. Claim **11** is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's background in view of Nishikawa et al. ("A Data-Driven Implementation of Telecommunication Network Systems," Proceedings of the Third International Symposium on Autonomous Decentralized Systems, IEEE, pp. 51-58, Apr. 1997).

32. In regard to claim 11:

33. The Applicant's background differs from the present invention because it does not disclose that a plurality of routers are combined.

34. Nishikawa et al. teaches in fig. 6(a) a plurality of routers that are combined in one node unit of an entire 2-dimentional network. This is done because there is a limitation on the number of ports of a router and hence as 6 input/output ports are required (col. 11, lines 15-17), the 2 routers are combined as shown. Also they are further combined

through their input/output ports when joined in the 2-dimentional network (fig. 6(d), fig. 6(f) and 6(h)).

35. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine a plurality of routers by joining the input/output ports of the routers.

36. One would have been motivated to do so to make a processing node unit of a network and hence further increase processing capabilities without having to increase the number of ports and hence cost and size of the router.

Conclusion

37. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty, which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections. See 37 CFR § 1.111.

a. Biagi ("The internal bottleneck: Terabit switch routers are coming of age," http://telephonyonline.com/ar/telecom_internal_bottleneck_terabit/, 12/7/1998) teaches that the router becomes the bottleneck of the network when running

slower than the network speeds and that faster routers are required in order to match the bandwidth requirements of the network.

b. Terada et al. (US004907187) teach a data driven processor.

c. Iwashita (US004591979) teaches another data driven processor.

d. Dennis (US004814978) teaches a data flow processor and also details a 2x2 router network in fig. 25.

e. L3 Communications ("PCM Tutorial, Time Division Multiplexing," http://www.l-3com.com/TE/tech/pcm3.html, 3/20/2000) teaches the fundamentals of TDM and shows how the sample rate has to be higher than the incoming transfer rates.

38. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amol V. Gole whose telephone number is 703-305-8888. The examiner can normally be reached on 9:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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